

Application No. 10/050,233
Amendment dated January 19, 2006
Reply to Office Action of October 5, 2005

Docket No. CM03359J

REMARKS/ARGUMENTS

The claims were amended by rewriting claims 11, 15, 34, 38, 40, 49, 52, 56 and canceling claim 53 without prejudice or disclaimer. Claims 3-5, 8-11, 13, 14, 15, 17-19, 34, 36-39, 40, 42-48, 49, 52, 54-60, 71, 73 and 75-80 remain in the application. Reconsideration of this application is requested.

Claim Objections:

Claim 38

Applicants have amended claim 38 to overcome the dependency issue noted by the Examiner. Applicants respectfully request that the objection now be withdrawn.

Claim 71

The Examiner objected to claim 71 stating that the wording was a substantial duplicate of claim 73. However, Applicants respectfully point out that claim 71 recites a frequency modulated output signal, while claim 73 recites an amplitude modulated output signal. Claim 71 recites the step of integrating the modulating signal whereas claim 73 lacks the step of integration. Applicants respectfully request that the objection to claim 71 be withdrawn.

Claim Rejections – 35 U.S.C. 112

Claims 11, 15, 34, 40 and 49 were rejected under 35 USC 112, second paragraph.

Applicants have amended each claim 11, 15, 34, 40 and 49 to more clearly recite the connection between the delay line and the tap selection circuit. The claims, as amended, are believed to overcome the rejection. Claim 56, though not rejected, has been similarly amended.

Application No. 10/050,233
Amendment dated January 19, 2006
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Docket No. CM03359J

Claim Rejections – 35 U.S.C. 103

Claim 3-5 were rejected under 35U.S.C. 103(a) as being unpatentable over Bockelman (20020110211) in view of Nakase et al (US Pub. No. 20020059352).

Applicants respectfully traverse the rejection. Neither reference taken individually or combined teaches that which is claimed by Applicants' invention. Applicants assert that the Nakase reference is not applicable to the invention at hand. The Nakase reference is directed towards digital processing that provides a filtering function of digital signals. The very fact that Nakase provides filtering means that the output contains a subset of signals from the input. Nakase sums (40) amplitude scaled delayed versions of a digitized input signal. Thus, in Nakase, no new frequency domain signals are generated at the output that were not already in existence at the input. Applicants' invention, on the other hand, provides a modulated signal – a modulated signal is the creation of a frequency domain signal that is not present at the input. Each independent claim of Applicants' invention recites a modulator combining first and second output signals to produce a modulated output signal. There is no teaching or suggestion of Nakase of providing a modulator. The filtering function of Nakase cannot be interpreted as a modulator – to do so would be like equating a decoder to an encoder.

Another distinction between Nakase and Applicants' invention the selectors of Nakase (for example FIG. selectors 20, 21) have independent inputs – the selectors are not connected in parallel. In Applicant's invention, the structure as claimed in independent claim 3, 4 and 5, creates a structure in which the tap selectors are in parallel. The selectors of Nakase can never pick the same tap at the same time. In Applicants' invention, it is possible for the structure as claimed, to pick the same tap at the same time because the tap selectors are in parallel. In view of the above arguments it would not be obvious to combine Nakase with Bockelman and even if the references were combinable the combination would not produce that which is claimed by applicants' invention.

Accordingly the rejection of claims 3-5 is believed to be overcome.

Application No. 10/050,233
 Amendment dated January 19, 2006
 Reply to Office Action of October 5, 2005

Docket No. CM03359J

Claim Rejections – 35 U.S.C. 102(e)

Claim 49 was rejected under 35 U.S.C. 102(e) as being anticipated by Nakase et al (US Pub. No. 2002/0059352).

Applicants respectfully traverse the rejection. As discussed above, Nakase teaches a digital filter. Nakase fails to teach or suggest the step of modulating. A filtered output will always produce a subset of the original input. Modulating two signals generates new frequency output. The rejection of claim 49 is thus overcome.

Claim Rejections – 35 U.S.C. 102(e)

Claim 11, 13-14, 15, 17-19, 52-55, 56, 59-60 under 35 U.S.C. 102(e) as being anticipated by Juan et al (US Pub. No. 2003/0099321).

Applicants respectfully amend in part and traverse in part.

Claim 11 recites: “a first multiplexer and a second multiplexer, wherein the first sequence of tap addresses C_{ja} are applied to the first multiplexer to produce a first output signal F_{outa} , and wherein the second sequence of tap addresses C_{jb} are applied to the second multiplexer to produce a second output signal F_{outb} ” Thus, Applicants’ multiplexers are independently controlled from each other. Juan, on the other hand, drives the input of the second multiplexer with an output from the first multiplexer – thus the output of one is feeding the input of the other.

Claim 15 recites: “... a first multiplexer, wherein the sequence of tap addresses C_{ja} are applied to a plurality of inputs of the first multiplexer to produce a first output signal F_{outa} ; a second multiplexer, wherein the sequence of tap addresses C_{jb} are added to a delay factor $\alpha/(2\pi)$ where α is a desired phase shift in radians and applied to a plurality of inputs of the second multiplexer to produce a second output signal F_{outb} .” Again, Juan feeds the output of the first multiplexer (250) into the taps (270) that control the second multiplexer (274) – as opposed to the two multiplexers being controlled independently.

Claim 52, as amended, incorporates the elements of claim 53, now canceled. Claim 53 recites: “applying the first sequence of tap addresses C_{ja} to a first multiplexer to produce a first output signal F_{outa} ; and applying the second sequence of tap addresses C_{jb} to a second multiplexer to produce a second output signal F_{outb} ,” Again, the output of Applicants first multiplexer is not being fed to the input of the taps and second multiplexer as is done in Juan.

Application No. 10/050,233
Amendment dated January 19, 2006
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Docket No. CM03359J

Claim 56, as amended, recites the step of: "selecting a sequence of tap addresses C_{ja} from the delay locked loop having the plurality of addressable delay line tap outputs;" The delay line of Applicants' claim 56 provides all of the plurality of addressable delay line tap outputs. Juan uses two sets of delay lines (24) and (270) with two sets of tap outputs (M) and (S) as shown in FIG. 7. Claim 56, recites the step of: "applying the sequence of tap addresses C_{ja} to a plurality of inputs of a first multiplexer to produce a first output signal F_{outa} ; and applying the sequence of tap addresses C_{ja} to a plurality of inputs of a second multiplexer to produce a second output signal F_{outh} ". As discussed above, the output of Applicants' first multiplexer is not being fed to the input of a second set of taps that control a second multiplexer as is done in Juan.

Accordingly, the rejection of independent claims 11, 15, 52 and 56, as amended, is overcome. Claims 13, 14, 17-19, 53-55, and 59-60 are dependent claims providing further limitations to what are believed to be allowable claims and hence are also in condition for allowance.

Allowed Claims:

Claims 8-10, 79 and 80 are allowed.

Applicants thank the Examiner for the allowance of claims 8-10, 79 and 80.

Allowable subject Matter:

The Examiner indicated that claims 34, 40 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph.

As discussed above, claims 34 and 40 have been amended to overcome the rejection and claims 34 and 40 are now believed to be in condition for allowance.

The Examiner indicated that claims 71 and 73 would be allowable if rewritten or amended to overcome the objection set forth in the office action.

Applicants believe that the discussion presented above has overcome the objection to claim 71. Thus, both claims 71 and 73 are believed to be in condition for allowance.

Application No. 10/050,233
Amendment dated January 19, 2006
Reply to Office Action of October 5, 2005

Docket No. CM03359J

The Examiner indicated that claims 36-39, 42-48, 57-58 and 75-78 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Claims 36-39 depend on and provide further limitations to what is now believed to be an allowable claim 34, and hence are also in condition for allowance.

Claims 42-48 depend on and provide further limitations (directly or indirectly) to what is now believed to be an allowable claim 40, and hence are also in condition for allowance.

Under item 12 of the Office Action dated Oct. 5, 2005, Applicants note that the Examiner requested that claim 9 be rewritten to overcome all objections. This was done in the previous amendment, and claim 9 has been indicated as being allowed by the Examiner. Thus, Applicants assume that this text pertaining to claim 9 was inadvertently placed in this Office Action and have not amended claim 9 any further.

Accordingly, claims 8, 9, 10, 79, 80, 34, 40, 71, 73, 36-39, 42-48, 57, 58, 75-78 are all believed to be in condition for allowance.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

The Applicants believe that the subject application, as amended, is in condition for allowance. Such action is earnestly solicited by the Applicants.

In the event that the Examiner deems the present application non-allowable, it is requested that the Examiner telephone the Applicant's attorney or agent at the number indicated below so that the prosecution of the present case may be advanced by the clarification of any continuing rejection.

Application No. 10/050,233
Amendment dated January 19, 2006
Reply to Office Action of October 5, 2005

Docket No. CM03359J


The Commissioner is hereby authorized to charge Deposit Account 502117, Motorola, Inc, with any fees which may be required in the prosecution of this application.

Respectfully submitted,

January 19, 2006

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